AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A semiconductor device, comprising:

a plurality ~~number~~ of spaced apart through electrodes with equal cross-sectional areas in a semiconductor chip linking a front surface to a back surface thereof, ~~the number of the through electrodes being determined according to a magnitude of an electric current with respect to an identical signal.~~

a first number of adjacent ones of the plurality of through electrodes being electrically connected to one another to form a power-supply through electrode which links the front and back surfaces of the chip and is in communication with a power supply, a second number of adjacent ones of the plurality of through hole electrodes being electrically connected to one another to form a grounding through electrode which links the front and back surfaces of the chip and is in communication with ground, and wherein only one of the plurality of through electrodes is used to form a particular signal-routing through electrode; and

wherein at least one of the first number and the second number is two or greater, so that at least one of the power-supply through electrode and the grounding through electrode is made up of at least two adjacent ones of the through electrodes which are electrically connected to one another, whereas the signal-routing electrode is made up of only one of the through electrodes.

2. (Original) The semiconductor device as set forth in claim 1, wherein at least one type of the through electrodes is contact through electrodes electrically connected to that semiconductor chip.

3. (Original) The semiconductor device as set forth in claim 1, wherein at least one type of the through electrodes is non-contact through electrodes not electrically connected to that semiconductor chip.

4. (Currently amended) The semiconductor device as set forth in claim 1, wherein wherein both of the first number and the second number is two or greater, so that each of the power-supply through electrode and the grounding through electrode is made up of at least two adjacent ones of the through electrodes which are electrically connected to one another, whereas the signal-routing electrode is made up of only one of the through electrodes. ~~a number of those through electrodes which are connected to a ground terminal or a power supply terminal of the semiconductor chip is greater than a number of those through electrodes which are connected to a signal terminal thereof~~.

5. (Currently amended) A chip-stack semiconductor device, comprising multiple stacked semiconductor chips, each of the semiconductor chips including a semiconductor device according to claim 1. ~~number of through electrodes with equal cross-sectional~~

~~areas therein linking a front surface to a back surface thereof, the number of the through electrodes being determined according to a magnitude of an electric current with respect to an identical signal.~~

6. (Currently amended) A chip-stack semiconductor device, comprising:

~~multiple~~ a plurality of stacked semiconductor chips, each of the semiconductor chips including a number of through electrodes with equal cross-sectional areas therein linking a front surface to a back surface thereof, ~~the number of the through electrodes being determined according to a magnitude of an electric current with respect to an identical signal, wherein~~

wherein at least one of a power-supply through electrode connected to a power supply and a grounding through electrode connected to ground is made up of at least two adjacent ones of the through electrodes which are electrically connected to one another, whereas a signal-routing electrode is made up of only one of the through electrodes, and

at least one type of the through electrodes is contact through electrodes electrically connected to that semiconductor chip.

7. (Currently amended) A chip-stack semiconductor device, comprising:

~~multiple~~ a plurality of stacked semiconductor chips, each of the semiconductor chips including a number of through electrodes with equal cross-sectional areas therein linking a front surface to a back surface thereof, ~~the number of the through electrodes~~

~~being determined according to a magnitude of an electric current with respect to an identical signal, wherein~~

wherein at least one of a power-supply through electrode connected to a power supply and a grounding through electrode connected to ground is made up of at least two adjacent ones of the through electrodes which are electrically connected to one another, whereas a signal-routing electrode is made up of only one of the through electrodes, and

at least one type of the through electrodes is non-contact through electrodes not electrically connected to that semiconductor chip.

8. (Currently amended) A chip-stack semiconductor device, comprising multiple stacked semiconductor chips, each of the semiconductor chips including a number of through electrodes with equal cross-sectional areas therein linking a front surface to a back surface thereof, the number of the through electrodes being determined according to a magnitude of an electric current with respect to an identical signal,

wherein

a number of adjacent connected ones of the ~~those~~ through electrodes which are connected to a ground terminal and/or a power supply terminal of that semiconductor chip is greater than a number of adjacent connected ones of the ~~those~~ through electrodes which are connected to a particular signal terminal thereof.

9. (Original) The chip-stack semiconductor device as set forth in claim 5, wherein a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

10. (Original) The chip-stack semiconductor device as set forth in claim 6, wherein a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

11. (Original) The chip-stack semiconductor device as set forth in claim 7, wherein a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

12. (Original) The chip-stack semiconductor device as set forth in claim 8, wherein a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

13. (Original) The chip-stack semiconductor device as set forth in claim 5, wherein the number of the through electrodes is increased according to an interconnect line length through the multiple stacked semiconductor chips.

14. (Original) The chip-stack semiconductor device as set forth in claim 6, wherein the number of the through electrodes is increased according to an interconnect line length through the multiple stacked semiconductor chips.

15. (Original) The chip-stack semiconductor device as set forth in claim 7, wherein the number of the through electrodes is increased according to an interconnect line length through the multiple stacked semiconductor chips.

16. (Original) The chip-stack semiconductor device as set forth in claim 8, wherein the number of the through electrodes is increased according to an interconnect line length through the multiple stacked semiconductor chips.

17. (Original) The chip-stack semiconductor device as set forth in claim 13, wherein the number of the through electrodes is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips.

18. (Original) The chip-stack semiconductor device as set forth in claim 14, wherein the number of the through electrodes is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips.

19. (Original) The chip-stack semiconductor device as set forth in claim 15, wherein the number of the through electrodes is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips.

20. (Original) The chip-stack semiconductor device as set forth in claim 16, wherein the number of the through electrodes is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips.

AMENDMENTS TO THE DRAWINGS

The attached sheets of drawings includes changes to Figs. 15-17. These sheets, which include Figs. 15-17, replace the original sheets including Figs. 15-17. In particular, Figs. 15-17 have been labeled "prior art."

Attachment: Replacement Sheets (3)